WHAT IS CLAIMED IS:

1. A rake receiver having a plurality of demodulating paths for demodulating symbols, the rake receiver comprising:

a memory storage block for storing corresponding demodulated symbols from each of the plurality of demodulating paths; and

storage control circuitry connected to each of the plurality of demodulating paths for receiving the demodulated symbols and for controlling the storage of the demodulated symbols within the memory storage block.

2. The rake receiver according to Claim 1, further comprising readout control circuitry connected to the memory storage block for controlling the reading out of the stored demodulated symbols.

3. The rake receiver according to Claim 1, further comprising a phase compensator connected to the storage control circuitry for phase compensating the demodulated symbols corresponding to each of the plurality of demodulating paths prior to storage of the demodulated symbols within the memory storage block.

4. A rake receiver having a plurality of demodulating paths for demodulating symbols, the rake receiver comprising:

storage control circuitry connected to each of the plurality of demodulating paths for receiving the demodulated symbols; and

a phase compensator connected to the storage control circuitry for receiving the demodulated symbols corresponding to each of the plurality of demodulating paths and for phase compensating the demodulated symbols.

5. The rake receiver according to Claim 4, further comprising a memory storage block for receiving the phase compensated, demodulated symbols corresponding to each of the plurality of demodulating paths and storing the demodulated symbols in accordance to signals received from the storage control circuitry.

6. The rake receiver according to Claim 5, further comprising readout control circuitry connected to the memory storage block for controlling the reading out of the stored demodulated symbols.

7. A rake receiver having a plurality of demodulating paths for demodulating symbols, the rake receiver comprising:

a phase compensator for receiving the demodulated symbols corresponding to each of the plurality of demodulating paths and for phase compensating the demodulated symbols; and

a memory storage block for storing the phase compensated, demodulated symbols corresponding to each of the plurality of demodulating paths.

8. A resource sharing rake receiver comprising:

an antenna for receiving signals;

a digital conversion block for converting the received signals to digital data;

a plurality of demodulating paths for demodulating symbols within the digital data, wherein each demodulating path includes at least a PN despreading block, and a Walsh decovering block;

a common memory storage block for storing corresponding demodulated symbols from each of the plurality of demodulating paths;

storage control circuitry connected to each of the plurality of demodulating paths for receiving the demodulated symbols and for controlling the storage of the demodulated symbols within the common memory storage block according to write request signals received from each demodulating path; and

readout control circuitry connected to the common memory storage block for controlling the reading out of the stored demodulated symbols.

9. The rake receiver according to Claim 8, wherein the storage control circuitry includes a memory controller for determining whether one of a demodulated symbol and combined demodulated symbols stored in a memory location of the common memory storage block should be combined with a symbol processed by the

storage control circuitry and stored at the same memory location.

10. The rake receiver according to Claim 9, wherein the memory controller determines whether to combine one of the demodulated symbol and the combined demodulated symbols stored in the common memory storage block with the processed symbol according to whether the processed symbol corresponds to a next earliest demodulating path of the plurality of demodulating paths, wherein the next earliest demodulating path is the demodulating path which outputs a next earliest demodulated symbol from among a series of demodulated symbols.

11. The rake receiver according to Claim 10, wherein the memory controller controls the combining of the processed symbol with one of the demodulated symbol and the combined demodulated symbols stored in the common memory storage block by reading out one of the demodulated symbol and the combined demodulated symbols stored in the common memory storage block upon receiving a read request signal, combining the read out symbol(s) with the processed symbol, and storing the combined read out symbol(s) and the processed symbol at the same memory location.

12. The rake receiver according to Claim 8, wherein the storage control circuitry includes a memory controller for controlling the combining and storage of a series of demodulated symbols at the same memory location of the common memory storage block.

13. The rake receiver according to Claim 12, wherein the memory controller stores a first symbol of the series of demodulated symbols corresponding to an earliest demodulating path of the plurality of demodulating paths at the same memory location of the common memory storage block, reads out the first symbol upon receiving a read request signal, combines the first symbol with a second symbol of the series of demodulated symbols corresponding to a next earliest demodulating path of the plurality of demodulating paths, stores the combined first and second symbols at the same memory location of the common memory storage block, and repeats the process

until a last symbol of the series of demodulated symbols is received, such that the series of demodulated symbols are all combined and stored at the same memory location of the common memory storage block.

14. The rake receiver according to Claim 13, further comprising means for numbering each of the plurality of demodulating paths, if two or more demodulating paths are at the same position according to an arbitrary time period, for determining which of the two or more demodulating paths is the earliest demodulating path.

15. The rake receiver according to Claim 13, wherein the memory controller processes the read request signal and the write request signals according to a priority scheme, and wherein only one read or write request signal can be processed at any given time according to the priority scheme.

16. The rake receiver according to Claim 8, further comprising a priority decision block for determining the processing priority of the write request signals and sending at least one signal to the storage control circuitry indicative of the determined processing priority of the write request signals for storing symbols within the common memory storage block.

17. The rake receiver according to Claim 16, wherein the priority decision block includes a reference timing generator (RTG) for generating read request signals, determining the processing priority of the read request signals, and sending at least one signal to the storage control circuitry indicative of the determined processing priority of the read request signals for reading out symbols stored in the common memory storage block.

18. The rake receiver according to Claim 8, wherein the readout control circuitry comprises:

a symbol combiner for reading out the stored demodulated symbols from the common memory storage block and for combining the read out demodulated symbols;

and

a long code descrambler for combining the combined demodulated symbols with a long code.

19. The rake receiver according to Claim 18, wherein the readout control circuitry further comprises a power bit extractor for receiving the combined demodulated symbols from the symbol combiner and extracting the power bits.

20. The rake receiver according to Claim 8, wherein each demodulating path further includes a channel estimation and phase compensation block for receiving output signals from a respective Walsh decovering block, phase compensating the symbols within the output signals, and sending the phase compensated, demodulated symbols to the common memory storage block.

21. The rake receiver according to Claim 8, further comprising a phase compensator block connected to the storage control circuitry for receiving the demodulated symbols corresponding to each of the plurality of demodulating paths and for phase compensating the demodulated symbols prior to storing the demodulated symbols within the common memory storage block.

22. A resource sharing rake receiver comprising:

an antenna for receiving signals;

a digital conversion block for converting the received signals to digital data;

a plurality of demodulating paths for demodulating symbols within the digital data, wherein each demodulating path includes at least a PN despreading block, and a Walsh decovering block;

a common phase compensator block for receiving the demodulated symbols corresponding to each of the plurality of demodulating paths and for phase compensating the demodulated symbols;

a common memory storage block for storing corresponding phase compensated, demodulated symbols from each of the plurality of demodulating paths;

storage control circuitry connected to each of the plurality of demodulating paths for receiving the phase compensated, demodulated symbols and for controlling the storage of the phase compensated, demodulated symbols within the common memory storage block according to write request signals received from each demodulating path; and

readout control circuitry connected to the common memory storage block for controlling the reading out of the stored phase compensated, demodulated symbols.

23. The rake receiver according to Claim 22, wherein the storage control circuitry includes a memory controller for determining whether one of a demodulated symbol and combined demodulated symbols stored in a memory location of the common memory storage block should be combined with a symbol processed by the storage control circuitry and stored at the same memory location.

24. The rake receiver according to Claim 23, wherein the memory controller determines whether to combine one of the demodulated symbol and the combined demodulated symbols stored in the common memory storage block with the processed symbol according to whether the processed symbol corresponds to a next earliest demodulating path of the plurality of demodulating paths, wherein the next earliest demodulating path is the demodulating path which outputs a next earliest demodulated symbol from among a series of demodulated symbols.

25. The rake receiver according to Claim 24, wherein the memory controller controls the combining of the processed symbol with one of the demodulated symbol and the combined demodulated symbols stored in the common memory storage block by reading out one of the demodulated symbol and the combined demodulated symbols stored in the common memory storage block upon receiving a read request signal, combining the read out symbol(s) with the processed symbol, and storing the combined read out symbol(s) and the processed symbol at the same memory location.

26. The rake receiver according to Claim 22, wherein the storage control

circuitry includes a memory controller for controlling the combining and storage of a series of demodulated symbols at the same memory location of the common memory storage block.

27. The rake receiver according to Claim 26, wherein the memory controller stores a first symbol of the series of demodulated symbols corresponding to an earliest demodulating path of the plurality of demodulating paths at the same memory location of the common memory storage block, reads out the first symbol upon receiving a read request signal, combines the first symbol with a second symbol of the series of demodulated symbols corresponding to a next earliest demodulating path of the plurality of demodulating paths, stores the combined first and second symbols at the same memory location of the common memory storage block, and repeats the process until a last symbol of the series of demodulated symbols is received, such that the series of demodulated symbols are all combined and stored at the same memory location of the common memory storage block.

28. The rake receiver according to Claim 27, further comprising means for numbering each of the plurality of demodulating paths, if two or more demodulating paths are at the same position according to an arbitrary time period, for determining which of the two or more demodulating paths is the earliest demodulating path.

29. The rake receiver according to Claim 27, wherein the memory controller processes the read request signal and the write request signals according to a priority scheme, and wherein only one read or write request signal can be processed at any given time according to the priority scheme.

30. The rake receiver according to Claim 22, further comprising a priority decision block for determining the processing priority of the write request signals and sending at least one signal to the storage control circuitry indicative of the determined processing priority of the write request signals for storing symbols within the common memory storage block.

31. The rake receiver according to Claim 30, wherein the priority decision block includes a reference timing generator (RTG) for generating read request signals, determining the processing priority of the read request signals, and sending at least one signal to the storage control circuitry indicative of the determined processing priority of the read request signals for reading out symbols stored in the common memory storage block.

32. The rake receiver according to Claim 31, wherein the priority decision block includes a pending status state machine for receiving the write request and read request signals and registering the same according to their order of generation by causing transition of a corresponding write pending or read pending bit, respectively, to a logic one value, and wherein each write pending and read pending bit having a logic one value indicates a presently pending write or read request, respectively, to be processed.

33. The rake receiver according to Claim 32, wherein the priority decision block further includes a channel priority decision block and a demodulating path priority decision block for selecting a channel and a demodulating path from the plurality of demodulating paths, respectively, according to a priority scheme of the presently pending write and read requests.

34. The rake receiver according to Claim 33, wherein the priority decision block further includes a resource sharing state machine for receiving information about the selected channel and demodulating path and sending signals to the storage control circuitry for processing the presently pending write and read requests, and controlling the common memory storage block accordingly.

35. The rake receiver according to Claim 34, wherein the priority decision block further includes an acknowledgment signal generation logic block for receiving the signals from the resource sharing state machine, generating at least one

acknowledgment signal for at least the processed write and read requests corresponding to the presently pending write and read requests, and transmitting the at least one acknowledgment signal to the pending status state machine to indicate that the presently pending write and read requests have been processed, and wherein upon receipt of the at least one acknowledgment signal by the pending status state machine, the pending status state machine switches the corresponding write and/or read pending bits to a logic zero value.

36. The rake receiver according to Claim 35, wherein the at least one acknowledgment signal is also transmitted to write and read pointer controller blocks for increasing at least one corresponding write request pointer and at least one corresponding read request pointer, respectively, for processing a subsequent pending write and pending read request according to the priority scheme.

37. The rake receiver according to Claim 22, wherein the readout control circuitry comprises:

a symbol combiner for reading out the stored demodulated symbols from the common memory storage block and for combining the read out demodulated symbols; and

a long code descrambler for combining the combined demodulated symbols with a long code.

38. The rake receiver according to Claim 37, wherein the readout control circuitry further comprises a power bit extractor for receiving the combined demodulated symbols from the symbol combiner and extracting the power bits.

39. A priority decision block configured for a rake receiver, the priority decision block comprising:

means for controlling the processing of pending write and read requests for storing demodulated symbols to and reading out demodulated symbols from a memory storage block; and

means for sending at least one signal to a memory controller for controlling the storage and reading out of the demodulated symbols to and from the memory storage block in accordance with the processed pending write and read requests.

40. The priority decision block according to Claim 39, wherein the means for controlling the processing of pending write and read requests includes a pending status state machine for receiving write request and read request signals and registering the same according to their order of generation by causing transition of a corresponding write pending or read pending bit, respectively, to a logic one value, and wherein each write pending and read pending bit having a logic one value indicates one of the pending write and read requests, respectively, to be processed.

41. The priority decision block according to Claim 40, wherein the means for controlling the processing of pending write and read requests further includes a channel priority decision block and a demodulating path priority decision block for selecting a channel and a demodulating path from a plurality of demodulating paths of the rake receiver, respectively, according to a priority scheme of the pending write and read requests.

42. The priority decision block according to Claim 41, wherein the means for sending at least one signal to the memory controller includes a resource sharing state machine for receiving information about the selected channel and demodulating path and sending signals to at least the memory controller for processing the pending write and read requests, and controlling the memory storage block accordingly.

43. The priority decision block according to Claim 42, wherein the means for controlling the processing of pending write and read requests includes an acknowledgment signal generation logic block for receiving the signals from the resource sharing state machine, generating at least one acknowledgment signal for at least the processed write and read requests corresponding to the pending write and read requests, and transmitting the at least one acknowledgment signal to the pending status

state machine to indicate that the pending write and read requests have been processed, and wherein upon receipt of the at least one acknowledgment signal by the pending status state machine, the pending status state machine switches the corresponding write and/or read pending bits to a logic zero value.

44. The priority decision block according to Claim 43, further comprising write and read pointer controller block for receiving the at least one acknowledgment signal for increasing at least one corresponding write request pointer and at least one corresponding read request pointer, respectively, for processing a subsequent pending write and pending read request of the pending write and read requests according to the priority scheme.